An Analytical Design Approach for Inverter Output Impedance in Parallel Operation of Micro Source Inverters

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Abstract *– This paper proposes an analytical framework to design an inverter output impedance in microgrid applications to meet the requirements of proportional load sharing and low total harmonic distortion in the output voltage. In the proposed work, an integral controller is designed in order to make the overall impedance of an inverter to be capacitive in nature. The optimum design of overall capacitive impedance at the harmonic frequencies ensures low THD levels in the output voltage without affecting proportional load sharing, which is determined by an inverter impedance at fundamental frequency component. The output impedance design decouples to meet different requirements at the same time. The focus is also laid on inherent limitations of conventional droop control of inverters and its remedial measures through bolting regulator on its control loop. A multilevel VRI topology is proposed and its parameters/coefficients are optimized. Small signal stability analysis is performed to ensure steady state stable operation. The load voltage THD is evaluated through FFT tool for parallelly operated C inverters feeding a nonlinear load to prove the effectiveness of the proposed design through time domain simulations.*

Keywords— Power Sharing, Power Quality, Stability, Total Harmonic Distortion.

1. INTRODUCTION

When an idea of the microgrid emerged first near around 2000, it was suggested as a way to integrate renewable energy sources. These energy sources are subjected to volatility and intermittentness, and their availability is not constant. Consequently, their inability to be connected in significant quantities gave rise to the concept of the microgrid. However, because of their ability to regenerate themselves over time and the deterioration and depletion of the global environment and energy supply, renewable energy resources have drawn a lot of attention recently. Power system engineers require the integration of distributed energy resources based on renewable energy to meet the goals of a carbon-free, affordable, and reliable supply[1-3]. Power electronic-based converters are used to interface the majority of these resources with the utility grid and/or local load. The quality of load voltage, delivered by an inverter may depend on number of factors. Possibly, one of them is output impedance that has a significant impact on quality of the output voltage. The overall harmonic distortion of the output voltage varies depending on whether an inverter is configured with an inductive or resistive output impedance. Apart from this, an accurate load sharing is also required in conjunction with this power quality feature, and it is too governed by an inverter output impedance.

An islanded mode of operation in the microgrid is a challenging task as it itself is responsible for managing nominal system voltage and frequency. Under this mode of operation, output impedances of parallel connected multiple inverters play a crucial role in sharing active as well as reactive power to the load. Any mismatches in the output impedances of inverters cause different operating conditions at the point of common load and consequently affect the power sharing to the local load. This will lead to mismatches in harmonic current sharing and fundamental current component and ultimately reactive power. The management of inverter output impedance could be a solution for the above mentioned problem. In literature, this issue has been addressed widely and solved by introducing virtual impedance in the control loop. The objective of adding virtual impedance is to make per unit output impedance of each inverter equal[4-7]. The nature of the output impedance may be resistive, inductive, resistive-inductive and resistive-capacitive and it should be carefully selected while applying it. Normalizing the output impedances of multiple inverters will not work as line impedances may also have different values.

Droop controllers allow power inverters to exchange reactive and active power with grid and/or load. However, the intrinsic drawbacks of the typical droop controller include erroneous power sharing as a result of noise, disturbances, numerical computations, mismatched components, etc [8-12].

Parallel functioning of inverters becomes crucial when it comes to the availability of high current power electronic equipment, system redundancy, the reliability required by crucial customers, etc. As a result, it is important to properly handle the problem of distributing the load across inverters operating in parallel. Through parallel operation, the problems with thermal management and high power in inverters are meant to be resolved[13-14].

Researchers have previously examined and used the mechanism of droop control to regulate both active and

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reactive power, as well as how it affects frequency and voltage. The negligible inertia of renewable energy sources, however, calls for greater attention to inverter control. Researchers pertaining to this area have conducted a thorough investigation of this field in the recent past. In hierarchical control structure, the droop technique is typically employed to enable the concurrent operation of several voltage source inverters sharing loads and confirming power quality standards. By making control over voltage amplitude and frequency, the primary layer adds virtual inertia, which replicates the inertial characteristics of traditional power systems and guarantees accurate power distribution among the inverters. The second layer of control corrects frequency and the voltage amplitude variations brought on by the droop equations [15-21].To reduce the inherent temporal gap between primary and secondary control, a new data-driven distributed control structure for voltage/frequency regulation & reactive/active power sharing of isolated microgrids is proposed in [22]. This structure uses a droop-free paradigm. [23] focuses on a way to use regulators in place of secondary control and primary droop control. In [24], a method for enhancing the quality of load voltage in droop-controlled islanded microgrids using appropriately tuned inner controllers is proposed. Adding a virtual impedance loop instead of an inner controllers has also been demonstrated to further reduce distortion at the PCC of the local load.

1.1 Objectives

Keeping in view the research work described above, the following objectives are achieved in this paper:

i. To describe the mechanism behind deterioration of load voltage and its dependency on inverter output impedance.
ii. To design capacitance in C type inverter through analytical approach fulfilling the requirements of proportional load sharing and low THD in load voltage.
iii. To introduce VRI topology for different levels and procedure to optimize its coefficients.

Section 2nd describes the deterioration mechanism of the output voltage of a single phase inverter. Parameter of C type single phase inverter is designed in the section 3rd. VRI topology is proposed in the section 4th followed by result and discussion in the section 5th. At last, paper is concluded in the section 6th.

2. DETERIORATION MECHANISM OF VOLTAGE

The output voltage of an inverter shown in Figure.1 is given as [5]-

$$V_o = V_r - i\,Z_o(s) \quad (1)$$

The current *i* contains harmonics due to the presence of nonlinear load or/and the PWM phenomena in the inverter thus causing harmonic voltage drop in an impedance, Z_o. Components of harmonic voltage appearing in the output voltage will degrade the output voltage and induces total harmonic distortion. THD may also appear in the output voltage due to harmonic components in the voltage reference V_r .

2.1 Impact of Z_o

The inverter current *i* and its harmonic components can be written as [7] –

$$i = \sqrt{2}\sum_{h=1}^{\infty} I_h \sin(h\omega t + \Phi_h) \quad (2)$$

The fundamental component of v_o is-

$$v_1 = V_r - |Z_o(j\omega)|\sqrt{2}\, I_1 \sin(\omega t + \Phi_1 + \theta) \quad (3)$$

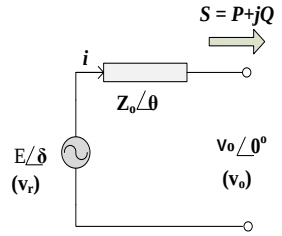


Fig. 1. Inverter model.

Where V_r, reference voltage is

$$V_r = \sqrt{2}\, E \sin(\omega t + \delta) \quad (4)$$

therefore, $$v_1 = \sqrt{2}\, V_1 \sin(\omega t + \beta_o) \quad (5)$$

Where

$$V_1 = \sqrt{(E^2 + I_1^2 |Z_o(j\omega)|^2 - 2\,E\,I_1 |Z_o(j\omega)| \cos(\Phi_1 + \theta - \delta))} \quad (6)$$

and $$\beta_o = \tan^{-1}\left(\frac{I_1 |Z_o(j\omega)| \sin(\Phi_1 + \theta - \delta)}{I_1 |Z_o(j\omega)| \cos(\Phi_1 + \theta - \delta) - E}\right) \quad (7)$$

Now the output voltage harmonic components would be-

$$v_h = v_{hmax} \sin(h\omega t + \Phi_h + \angle Z_o(jh\omega)) \quad (8)$$

Where $v_{hmax} = \sqrt{2}\sum_{h=2}^{\infty} I_h |Z_o(jh\omega)|$

From (8), it is seen that v_h depends upon harmonic current components and Z_o (at harmonic frequency components). Through this analysis, it is evident that v_h is not affected by v_1 and this feature can be used to design the impedance for different purposes. For a selected value of capacitance, the Z_o at harmonic frequencies can be reduced in order to improve THD of load voltage as described in (9). On the other hand objective of proportional load sharing is governed by fundamental component of an inverter output impedance [5-7].

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} |Z_o(jh\omega)|^2 I_h^2}}{V_1} \quad (9)$$

3. DESIGN OF C INVERTERS

Single phase inverter circuit shown in Figure.2 is under consideration for designing the capacitive output impedance. An inverter is connected to the AC bus through a switch where load is assumed to be connected.

The current *i* through inductor can be passed through an integrator block to make the output impedance

to be capacitive. This is shown as a closed loop system in Figure.3 [5,6].

The following two equations are deduced from Figure.2 and Figure.3 and written as-

$$u = \mathbf{v_r} - \frac{1}{sC_0} i \quad \text{and} \quad u_f = sLi + v_o \tag{10}$$

Equating u and u_f in (10) yields-

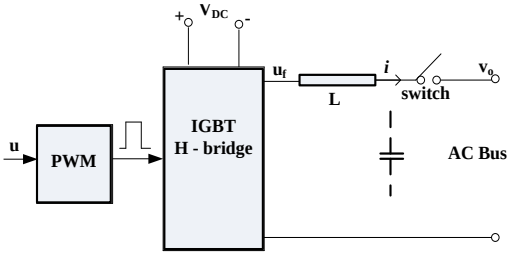


Fig. 2. Physical implementation of single phase inverter.

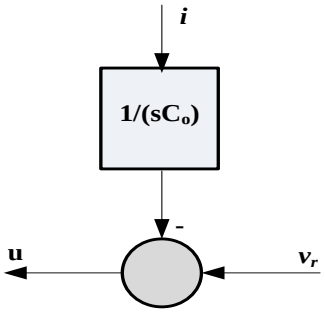


Fig. 3. Controller for achieving capacitive output impedance.

$$v_o = v_r - i\, Z_o\,(s) \tag{11}$$

Where $Z_o(s) = \frac{1}{sC_o} + sL$

$Z_o(s) \approx \frac{1}{sC_o}$ (if capacitor C_o is chosen small enough)

3.1 Analytical Design Process

As stated earlier, the distortion (THD) of the voltage is governed by inverter Z_o at harmonic frequencies. The procedure of designing C_o or integrator constant is given below [7,8].

$$|Z_o(jh\omega^*)|^2 = (h\omega^* L - \frac{1}{h\omega^* C_o})^2 \tag{13}$$

h and ω^* are harmonic order and fundamental frequency respectively. L being the filter inductance, minimization of the following expression ensures improved THD for a particular virtual capacitor C_o.

$$\min_{C_o} \sum_{h=2}^{\infty} I_{1h}^2 |Z_o(jh\omega^*)|^2 \tag{14}$$

Where $i = \frac{I_h}{I_1}$, h^{th} order normalized harmonic current with respect to fundamental current. Differentiating (14) with respect to C_o and equating to zero yields the optimum capacitance. The optimal capacitance

$$C_o = \frac{1}{(\omega^*)^2} \frac{1}{L} \frac{\sum_{h=2}^{N} \frac{i_{1h}^2}{h^2}}{\sum_{h=2}^{N} i_{1h}^2} \tag{15}$$

It is applicable to any a priori estimated harmonic distribution of current. Where i_{1h} is the normalized h^{th} harmonic current.

$$f(C_o) = (L\omega^*)^2 \sum_{h=2}^{N} i_{1h}^2 \left(h - \frac{1}{h} \frac{\sum_{h=2}^{N} i_{1h}^2}{\sum_{h=2}^{N} \frac{i_{1h}^2}{h^2}}\right)^2 \tag{16}$$

It is evident from the above equation that THD is proportional to an inductance L. A small inductance, L not only reduces the inductor size and cost but it also enables small integrator gain ($L \sim \frac{1}{C_o}$) to ensure the stable current loop.

Assuming odd harmonics (h = 3,5,7…) that are equally distributed, (15) will have the form-

$$C_o = \frac{1}{(\omega^*)^2} \frac{1}{L} \frac{\sum_{h=3,5,7.....N} \frac{1}{h^2}}{\sum_{h=3,5,7.....N} 1} \tag{17}$$

Assuming the 3rd and 5th harmonic components, the optimal capacitance in (17) is given by-

$$C_o = \frac{17}{225\,(\omega^*)^2 L} \tag{18}$$

3.2 Proportional Load Sharing

Besides low THD in the output voltage, the load sharing proportional to the power rating of inverters is to be carried out but the conditions for accomplishing this objective are not met in practicality. Therefore the idea of robust droop controller arises. In this section, the conditions of proportional load sharing for conventional droop controllers are derived first and then robust droop control is introduced. Figure.4 shows two inverters with capacitive output impedances connected in parallel. Feeder impedances are neglected and inverter output impedance dominates between inverter and the AC bus. In another Figure.5, single inverter is shown supplying power to another voltage source [7-12].

$$P = \left(\frac{EV_o}{Z_o}\cos(\delta) - \frac{V_o^2}{Z_o}\right)\cos(\theta) + \frac{EV_o}{Z_o}\sin(\delta)\sin(\theta) \tag{19}$$

$$Q = \left(\frac{EV_o}{Z_o}\cos(\delta) - \frac{V_o^2}{Z_o}\right)\sin(\theta) - \frac{EV_o}{Z_o}\sin(\delta)\cos(\theta)$$

For capacitive output, $\theta = -90^o$

$$P = -\frac{EV_o}{Z_o}\sin(\delta) \tag{20}$$

$$Q = -\frac{EV_o}{Z_o}\cos(\delta) + \frac{V_o^2}{Z_o} \tag{21}$$

For very small angle δ, P~ -δ & Q ~ -E

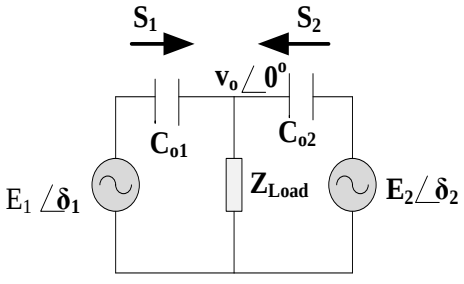


Fig. 4. C inverters operated in parallel.

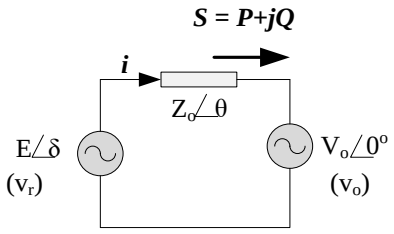


Fig. 5. Power delivered to voltage source.

Therefore conventional droop control scheme has the form and shown in Figure.6 [11-12].

$$E_i = E^* + n_i Q_i$$
$$\omega_i = \omega^* + m_i P_i \quad (22)$$

3.3 Reactive Power Sharing

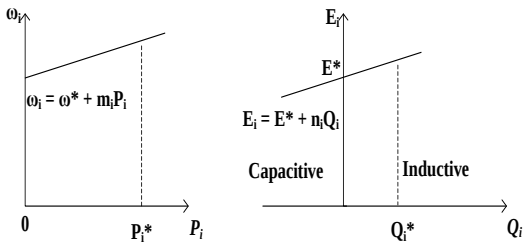


Fig. 6. Droop Control Strategy for C Inverter.

The expressions of reactive power for *i* (*i* = 1,2..) inverters are written as-

$$Q_i = \frac{-E^*\cos\delta_i + V_o}{n_i \cos\delta_i + \frac{Z_{oi}}{V_o}} \quad (23)$$

Substituting (23) into (22), the voltage amplitude deviation between two inverters is given by (24)-

$$\Delta E = E_2 - E_1 = \frac{-E^*\cos\delta_1 + V_o}{\cos\delta_1 + \frac{Z_{o1}}{n_1 V_o}} - \frac{-E^*\cos\delta_2 + V_o}{\cos\delta_2 + \frac{Z_{o2}}{n_2 V_o}} \quad (24)$$

Voltage deviation between two units lead to considerable error in power sharing. Therefore in order for $n_1Q_1 = n_2Q_2$ to hold, voltage deviation should be zero. However, in practicality ,this condition is not obeyed. It is satisfied if

$$\frac{n_1}{Z_{o1}} = \frac{n_2}{Z_{o2}} \text{ and } \delta_1 = \delta_2 \quad (25)$$

Therefore in order to achieve accurate reactive power sharing, capacitive output impedance should be designed to satisfy-

$$\frac{Z_{o2}}{Z_{o1}} = \frac{n_2}{n_1} = \frac{S_1}{S_2} \quad (26)$$

$$\frac{Z_{o2}S_2}{(E*)^2} = \frac{Z_{o1}S_1}{(E*)^2} \cdots\cdots \frac{Z_{on}S_n}{(E*)^2} \quad (27)$$

Where $S_1, S_2 \ldots S_n$ are inverter ratings respectively. From (27), it is evident that for achieving accurate reactive power sharing, the p.u output impedances of inverters should be same and this is the foundation of the approach known as virtual impedance. However it is difficult to get this in real scenario[7]. In the same way it can be shown that real power sharing can be ensured under the condition of $\frac{Z_{o2}}{Z_{o1}} = \frac{m_2}{m_1}$.

3.4 Robust Droop Control

The inherent problems of conventional droop control can be resolved by robust droop control through bolting a regulator onto its control loop as shown in Figure.7.

$$n_iQ_i + K_e (E^* - V_o) = 0 \quad (28)$$

If K_e is same for all inverters, the accurate reactive power sharing is guaranteed in proportion to the power rating of the inverters. At the steady state, input to the integrator is zero.

Therefore,

$$n_iQ_i = \text{constant} \quad (29)$$

The output voltage is given by

$$V_o = E^* + \frac{n_i}{K_e} Q_i = E^* + \frac{n_iQ_i}{E^* K_e} E^* \quad (30)$$

The output voltage can be maintained within a desired range by choosing large K_e thus achieving good voltage regulation [5-7].

4. VIRTUAL RESONANT IMPEDANCE TOPOLOGY

It has been shown earlier in section 2.1 that load voltage THD reduces significantly if Z_o of inverter is capacitive in nature. To further develop C inverter, the virtual resonant impedance is achieved as a control strategy to improve the load voltage quality.

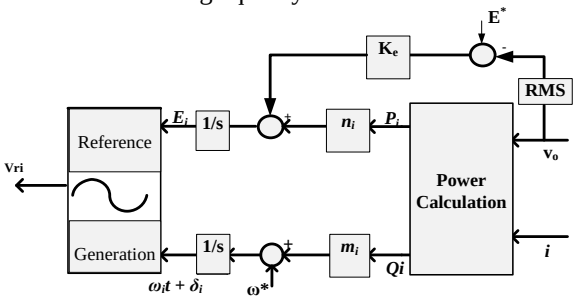


Fig. 7. Robust droop control.

Its foundation is a resonant impedance topology, shown in Figure.8, with capacitors and inductors, whose magnitude approaches zero at various frequencies. The suggested control approach incorporates the feedback of the inductor current through a transfer function. The VRI or transfer function coefficients are chosen and optimized to simultaneously lower load voltage harmonics of various orders, that minimize THD [7-12].

Table 1. Fundamental o/p Impedance at different levels.

VRI Level	Output impedance and its nature at s = jω
I Level	-j5.90 (capacitive)
II Level	-j7.16 ((capacitive)
III Level	-j8.11 (capacitive)
IV Level	-j9.08 (capacitive)

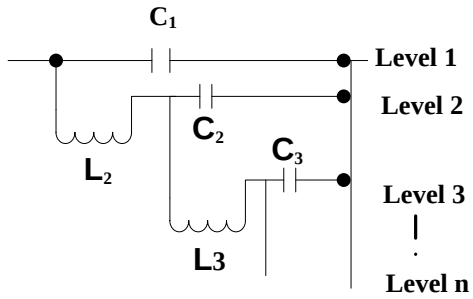


Fig. 8. VRI Topology.

Upon adding level 1 of the VRI, the inverter is actually a conventional C-inverter with $Z_d = \frac{1}{sC_1}$, where it is possible to design C_1 to lower the voltage harmonic component of a specific order (3rd in this case) with Z_d regarded as the virtual impedance. When two particular order (3rd and 5th) of harmonics are concerned, the virtual impedance can be described in (31) upon adding the levels 1 and 2 of the VRI topology.

$$Z_d = \frac{C_2 L_2 s^2 + 1}{s(C_1 + C_2 + C_1 C_2 L_2 s^2)} \quad (31)$$

Where C_1, C_2, L_2 are designed to improve voltage harmonics at two different order frequencies. Parameters of VRI can also be designed for n level in general.

4.1 Design of Three Level VRI

Three designated order harmonics might be addressed when the levels one, two and three of the VRI are added. If h_1, h_2 and h_3 order harmonic components are concerned, according to (33) , the numerator of the inverter's Z_o should be zero at concerned frequencies. (see A.4 in APPENDIX A). It is equivalent to-

$$(s^2 + h_1^2\omega^2)(s^2 + h_2^2\omega^2)(s^2 + h_3^2\omega^2)=0 \quad (32)$$

Inverter output impedance including the filter capacitor is given by (33).

$$Z_o = \frac{(sL + Z_d)}{sC(sL + Z_d)+1} \quad (33)$$

Z_d can be calculated from Figure.8.Therefore, the coefficients of three level VRI are computed as-

$$C_1 = \frac{h_1^2h_2^2 + h_1^2h_3^2 + h_2^2h_3^2}{3L\omega^2 h_1^2h_3^2h_2^2},$$

$$C_2 = \frac{h_1^2h_2^2 + h_1^2h_3^2 + h_2^2h_3^2}{3(L+L_2)\omega^2 h_1^2h_3^2h_2^2},$$

$$C_3 = \frac{h_1^2h_2^2 + h_1^2h_3^2 + h_2^2h_3^2}{3(L+L_2+L_3)\omega^2 h_1^2h_3^2h_2^2} \quad (34)$$

Where L_2 and L_3 are given by-

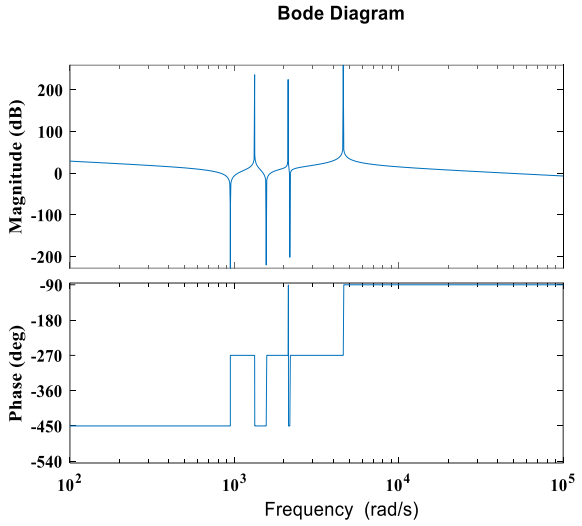
$$L_2 = \frac{K_2 - 3K_1 \pm \sqrt{(K_1+K_2)^2 - 16K_1}}{2(K_1 - K_2 + 2)} L,$$

$$L_3 = \frac{K_1 + K_2 \pm \sqrt{(K_1+K_2)^2 - 16K_1}}{2(K_1 - K_2 + 2)} L$$

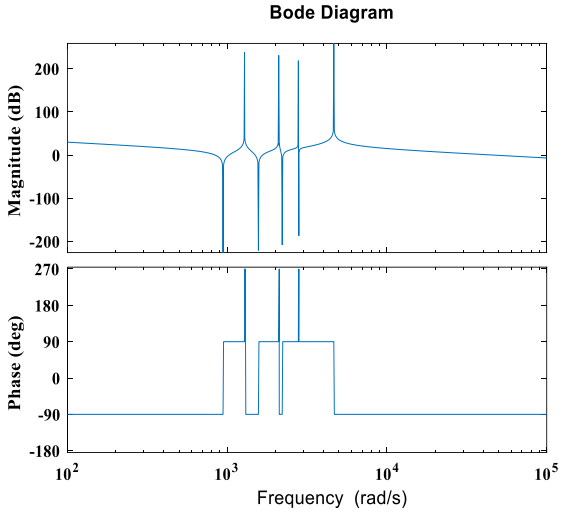
Where;

$$C_1.L = C_2.(L+L_2) = C_3.(L+L_2+L_3) = \frac{h_1^2h_2^2 + h_1^2h_3^2 + h_2^2h_3^2}{3\omega^2 h_1^2h_3^2h_2^2}$$

The calculation of the parameters requires values of K_1 and K_2 , and for that Appendix A can be referred. The output impedance magnitude and phase diagram of three level and four level VRI topology is shown in Figure.9. The fundamental frequency output impedance values for four levels of VRI topology are shown in Table.1.



(i)



(ii)

Fig. 9. Magnitude and phase diagram of inverter output impedance (i) three level (ii) four level VRI topology.

5. RESULT AND DISCUSSION

5.1 Small signal stability analysis

Small signal stability is conducted for one inverter participating in parallel operation. Small disturbance around phase angle (δ) and inverter RMS voltage (E) is considered in linearizing (19). V_o is the RMS output voltage across the load [5].

$$\Delta P(s) = V_o \frac{(\cos\delta\cos\theta + \sin\delta\sin\theta)}{Z_o}\Delta E(s) + \frac{E V_o(-\sin\delta\cos\theta + \cos\delta\sin\theta)}{Z_o}\Delta\delta(s) \quad (35)$$

$$\Delta Q(s) = V_o \frac{(\cos\delta\sin\theta - \sin\delta\cos\theta)}{Z}\Delta E(s) - \quad (36)$$

$$EV_o \frac{(\sin\delta \sin\theta+\cos\delta \cos\theta)}{Zo}\Delta\delta(s)$$

Linearizing controller Equations yields-

$$\Delta\omega(s) = m\Delta P(s) \;\; \& \;\; \Delta\omega(s) = s\Delta\delta(s) \qquad (37)$$

Normally both power components (Active & Reactive) are measured through low pass filter of the form $\frac{\omega_f}{s+\omega_f}$. Considering this point and using (35), (36) and (37) a fourth order polynomial is formed in δ to investigate the stability (refer Appendix A). It is evident from Figure.10 that the proposed strategy is stable for output impedance angle ranging from - $\frac{\pi}{2}$ to 0 rad.

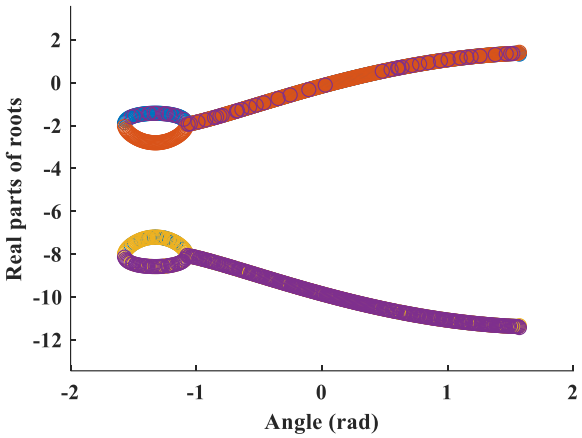


Fig. 10. Characteristics roots vs inverter output impedance angle.

5.2 C inverter simulation with nonlinear load

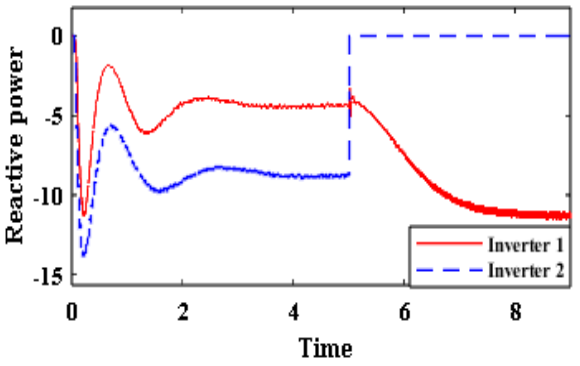
A system of two single phase C inverters operating in parallel is used to perform simulation for 9 sec to verify the design. Matlab Simulink R2022a software is used to carry out simulations on the system with processor AMD Ryzen 3 3250U and 8 GB ram. Initially inverter 2 (50 VA) and Inverter 1 (25VA) are operated in parallel to feed a nonlinear load (full bridge rectifier with LC filter, L = 150 µH and C = 1000 µF, R = 9Ω). At t = 5sec, inverter 2 is disconnected and only inverter 1 remains connected to the load. Detail parameters are given in Table 2.

Table.2 simulation parameters

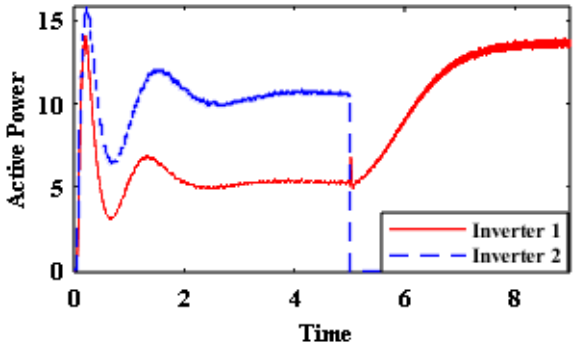
Parameters	value	Unit
F	50	Hz
V_{DC}	42	V
E*	12	V
f_s	7500	Hz
L	2.35	mH
ω*	314	rad/s
C	22	µF
K_e	20	
m_1	0.14	rad/W
m_2	0.07	rad/W
n_1	2.2	V/var
n_2	1.1	V/var

m (frequency-real power droop coefficient) and *n* (voltage- reactive power droop coefficient) are calculated from frequency boost ratio and voltage boost ratio respectively. Time domain responses are shown in Fig. 11. From Fig. 11(a), it is evident that both inverters shares power (P) in the ratio of 1:2 ($\frac{5.289}{10.470} \approx \frac{1}{2}$) during parallel operation. In the same time interval, reactive power (Q) also settles in the ratio of 1:2 ($\frac{-4.419}{-8.650} \approx \frac{1}{2}$). Steady state value of frequency is 50.33 Hz. All time domain waveforms are shown in Fig. 11 (i)-(viii) with the following units.

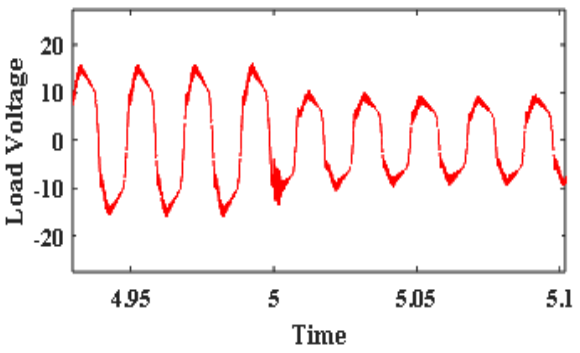
Reactive power- Var
Active power - Watt
Load voltage - Volt
Current- Amperes



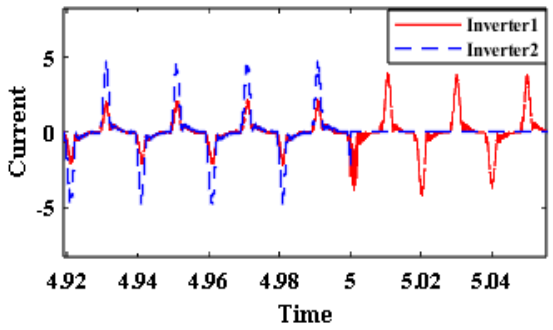
(i)



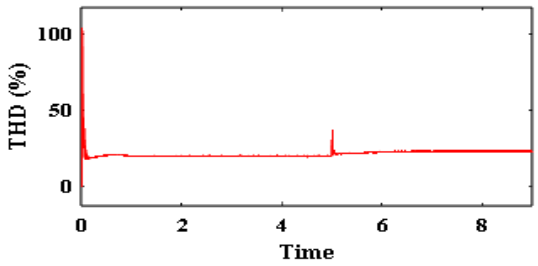
(ii)



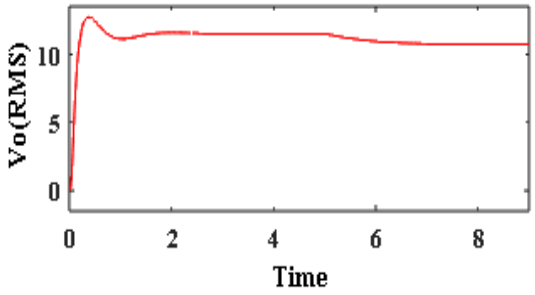
(iii)



(iv)



(v)



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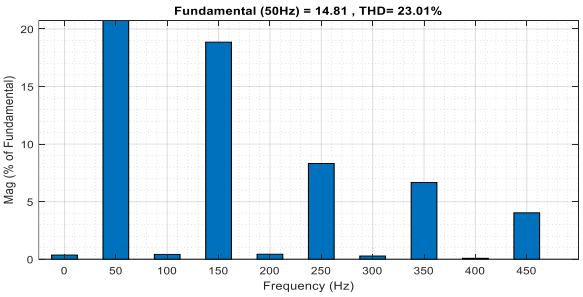
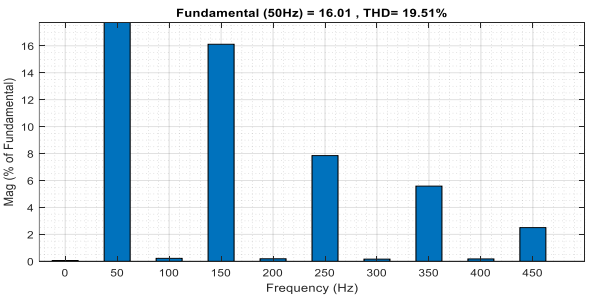


(vii)



(viii)

Fig 11 (i) Reactive power distribution vs time (ii) active power distribution vs time (iii) load voltage vs time (iv) Output current vs time (v) % THD in load voltage vs time (vi) Load voltage(RMS) vs time (vii) THD in load voltage when inverter 1 is operational (viii) THD in load voltage when both inverters are operational.

6. CONCLUSION AND FUTURE WORK

In this paper, an analytical approach is used to design integral controller parameter for C inverter in order to accomplish the objectives of proportionate power sharing among inverters and low total harmonic distortion in the output voltage. Inherent problems in the conventional droop control and its remedial measures are proposed as far as parallel operation of two inverters is concerned. In the next step, VRI topology is proposed for capacitive inverters with n levels in general to address different harmonics order in load voltage. Power sharing ratio of two parallel operated inverters is determined for a test example through time domain simulation. The procedural steps for obtaining optimized parameters for one, two and three levels of VRI topology are described. Small signal stability for any one inverter participating in the parallel operation is performed to ensure the stable operation

NOMENCLATURE

THD: Total Harmonic Distortion
FFT: Fast Fourier Transform
VRI: Virtual Resonant Impedance
p.u: per unit
o/p: output

REFERENCES

[1] IRENA 2017. Renewable capacity statistics. *International Renewable Energy Agency Abu Dhabi.*

[2] Saeed M. H, Fangzong W., Kalwar B. A. and Iqbal S., 2021. Review on Microgrids Challenges & Perspectives. *IEEE Access.* 9:166502-166517.

[3] Bhambri, S., Kumawat, M., Shrivastava, V., Agarwal, U., Jain N.K., 2023. The Energy Mix: An Emerging Trend in Distribution System. In: Singh, S.N., Jain, N., Agarwal, U., Kumawat, M. (eds) *Optimal Planning and Operation of Distributed Energy Resources. Energy Systems in Electrical Engineering*. Springer, Singapore, pp. 11-37.

[4] Tayab U. B., Roslan M.A.B., Hwai L. J. and Kashif M., 2017 A review of droop control techniques for rnicrogrid. *Renew. Sust. Energ. Rev.* 76:717-727.

[5] Bhambri S., Shrivastava V. and Kumawat M., 2023. Single Solution for Control and Synchronization of Inverters in Microgrids. *9th IEEE India International Conference on Power Electronics (IICPE)*,Sonipat, India, 28-30 November.IEEE.

[6] Zhong Q. C. and Zeng Y., 2013. Control of Inverters Via a Virtual Capacitor to Achieve Capacitive Output Impedance . *IEEE Transactions on Power Electronics*. 29(10):5568-5578.

[7] Zhong Q. C., 2013. Robust Droop Controller for Accurate Proportional Load Sharing Among Inverters Operated in Parallel .*IEEE Trans. Ind. Electron*. 60(4): 1281–1290.

[8] Lazzarin T. B., Bauer G.A.T. and Barbi I., 2013 A Control Strategy for Parallel Operation of Single-

Phase Voltage Source Inverters: Analysis, Design and Experimental Results . *IEEE Transactions On Industrial Electronics*. 60(6):2194-2204.

[9] Yao Z. and Xiao L., 2013. Control of Single-Phase Grid Connected Inverters With Nonlinear Loads . *IEEE Transactions on Industrial Electronics*, pp. 1384-1389.

[10] Chandorkar C M, Divan M D, and Adapa R, 1993 Control of Parallel Connected Inverters in Standalone ac Supply Systems. *IEEE Transactions On Industry Applications*. 29(1):136-143.

[11] Zhong Q. C and Zeng Y., 2016. Universal Droop Control of Inverters With Different Types of Output Impedance. *IEEE Access*. 4: 702-712.

[12] Zhong Q. C., Zeng Y. and Ren B., 2017. UDE-Based Robust Droop Control of Inverters in Parallel Operation. *IEEE Transactions on Industrial Electronics*, 64(9): 7552-7562.

[13] Tolani S. and Sensarma P., 2017. An Instantaneous Average Current Sharing Scheme for Parallel UPS Modules. *IEEE Transactions on Industrial Electronics*. 64 (12): 9210-9220.

[14] Rey J. M., Rosero C. X., Velasco M., Martí P., Miret J. and Castilla M., 2019. Local Frequency Restoration for Droop-Controlled Parallel Inverters in Islanded Microgrids. *IEEE Transactions on Energy Conversion*.34(3): 1232-1241.

[15] Han Y., Li H., Shen P., Coelho E. A. A., and Guerrero J. M., 2017. Review of active and reactive power sharing strategies in hierarchical controlled microgrids. *IEEE Trans. Power Electron*.32(3): 2427-2451.

[16] Mohammadi F. D., Vanashi Keshtkar H. K. and Feliachi A., 2018. State-space modeling analysis and distributed secondary frequency control of isolated microgrids .*IEEE Trans. Energy Convers*. 33: 155-165.

[17] Guo F., Wen C., Mao J. and Song Y. D., 2015. Distributed secondary voltage and frequency restoration control of droop-controlled inverter-based microgrids.*IEEE Trans. Ind. Electron.* 62(7): 4355-4364.

[18] Yuan W., Wang Y., Liu D., Deng F. and Chen Z., 2021. Efficiency-Prioritized Droop Control Strategy of AC Microgrid . *IEEE Journal of Emerging and Selected Topics in Power Electronics*.9, (3): 2936-2950.

[19] Han H., Hou X., Yang J., Wu J., Su M. and Guerrero J M., 2016. Review of Power Sharing Control Strategies for Islanding Operation of AC Microgrids. *IEEE Transactions on Smart Grid*. 7(1): 200-215 .

[20] Peng J. C-H. , Raman G., Soon J. L. and Hatziargyriou Nikos D., 2022. Droop Controlled Inverters as Educational Control Design Project . *IEEE Transactions on Power Systems*. 37(2): 1623-1633.

[21] S. Bhambri., V. Shrivastava., M. Kumawat and S. Agrawal., 2024. Modelling and Control of Microgrids in an Offgrid Operating Scenario: A Case Study. *IEEE Region 10 Symposium (TENSYMP)*, New Delhi, India, 27-28 September.IEEE.

[22] Zheng D. and Karimi A., 2020. Data driven distributed frequency/voltage and power sharing control for islanded microgrids. *IEEE Conference on Control Technology and Applications (CCTA)*. Montreal, QC, Canada. 1066-1071 24-26August.

[23] Nasirian V., Shafiee Q., Guerrero J. M., Lewis F. L. and Davoudi A., 2016. Droop-free distributed control for AC microgrids. *IEEE Trans. Power Electron*.31(2): 1600-1617.

[24] S. Bhambri., V. Shrivastava and M. Kumawat., 2024. Performance Improvement in Droop Controlled Islanded Microgrids via Selective Harmonic Control. *International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES)*. New Delhi, India, 26-28 April. IEEE.

APPENDIX A

$$s\Delta\delta(s)= m\frac{\omega_f}{s+\omega_f}\left(V_o\frac{(\cos\delta\cos\theta+\sin\delta\sin\theta)}{Zo}\Delta E(s) + \frac{E V_o(-\sin\delta\cos\theta+\cos\delta\sin\theta)}{Zo}\Delta\delta(s)\right) \quad A.1$$

$$s\Delta E(s) = \frac{\omega_f}{s+\omega_f}(n\Delta Q(s)) \quad A.2$$

A polynomial in δ is formed by substituting ΔE(s) in A.1.

$$A.s^4+B.s^3+C.s^2+D.s+F=0 \quad A.3$$

Where A, B, C, D and F are functions of inverter output impedance angle.

The numerator of Z_o is given by-

$$Ls^2(C_1+C_2+C_3+(C_1C_2L_2s^2)+(C_1C_3L_2s^2)+(C_1C_3L_3s^2)+(C_3C_2L_3s^2)+(C_1C_2C_3L_2L_3s^4))+(C_2L_2s^2)+(C_3L_2s^2)+(C_3L_3s^2)+(C_2C_3L_2L_3s^4)+1 \quad A.4$$

K_1 and K_2 are given by-

$$K_1 = \frac{27\,h_1^4h_2^4h_3^4}{h_1^2h_2^2+h_1^2h_3^2+h_2^2h_3^2} \quad A.5$$

$$K_2 = \frac{9\,h_1^2h_2^2h_3^2(h_1^2+h_2^2+h_3^2)}{h_1^2h_2^2+h_1^2h_3^2+h_2^2h_3^2} \quad A.6$$